REMARKS/ARGUMENTS

Prior to the present Amendment, Claims 1-11 were pending in the present application. Through this Amendment and Response, Applicant has amended Claim 1. No claims have been added or cancelled. Accordingly, following the entry of the present amendment, Claims 1-11 will be pending in the present application. Applicant notes with appreciation that Claims 4-5, 7-8, and 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. In the Office Action, Claims 1-3, 6 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mukainakano et al. (U.S. Patent No. 6,107,862). Applicant respectfully requests reconsideration of the rejection based on the above amendment and following remarks.

The charge pump circuit of the present invention, as claimed, includes "a delay circuit connected between the second terminal of the capacitor and the control terminal of the first transistor, wherein the delay circuit delays the first clock signal, which is provided to the control terminal of the first transistor, by a predetermined time and provides the delayed first clock signal to the second terminal of the capacitor." Such a delay circuit, as described in the specification (B1; Fig. 3), increases the voltage conversion efficiency. After a gate voltage (φT1) of a first transistor (TR1) is determined to be at a low level to turn off the first transistor, the delay circuit (B1) delays the determined voltage (φT1) and generates a delayed signal (φC1), thereby decreasing a voltage of the node (N1) between the first and second transistors (TR1, TR2) to the low level. That is, the voltage at the node (N1) changes after the gate voltage is determined to be at the low level. In other words, the node N1 voltage does not change during the period the gate voltage is decreasing, which prevents a large through current from being generated in the transistors (TR1, TR2).

Mukainakano does not teach or suggest the delay circuit of the present invention. In fact, Mukainakano teaches a device in which a large through current may be generated because of the following reasons:

In Fig. 7A of Mukainakano, when the switch (transistor) SW1 is turned off, the switch SW4 is turned on while the switch SW3 is being turned off, thereby providing a voltage V1 to the

capacitor C1 through the switch SW4 to increase the voltage at the node between the switches SW1 and SW2. In this case, a gate voltage signal A, which turns on the switch SW4, is not generated by delaying a gate voltage signal B, which turns off the switch SW1. Thus, the voltage at the node between the switches SW1 and SW2 may increase before the switch SW1 is surly turned off, which generates a large through current in the switch SW1. Accordingly, since Mukainakano does not disclose the delay circuit that delays a first clock signal, which is provided to the control terminal of the first transistor, by a predetermined time, Applicant submits that the present invention is not obvious over Mukainakano.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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